

# LC7522



3029A

SANYO SEMICONDUCTOR CORP

CMOS LSI

## Electronic Volume Control for Graphic Equalizer

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### Functions

- On-chip electronic volume control for graphic equalizer with 7 bands each of right/left
- 2dB/step variable in each band
- Maximum boost of +12dB, maximum cut of -12dB, and 13 positions in each band
- Simultaneous drive of right/left band
- Band setting by serial data input, 2 control lines
- CMOS LSI of 16V breakdown voltage

### Features

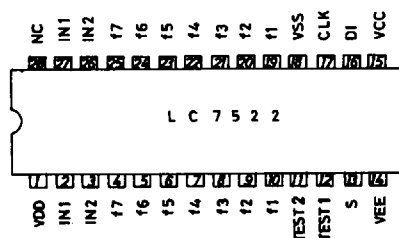
By using 3 chips of the LC7522, a controller (LC7060 or general-purpose microcomputer LC6502C), and a display LSI (LC7560→LCD, LC7565→FLT, LED), an electronic graphic equalizer system with the following features can be formed.

- The gain in each band can be increased/decreased with one touch.
- Since the preset memory contents can be called with one touch, your desired frequency characteristic to the music can be selected.  
(Example) User option 2 modes + maker option 3 modes + last channel memory
- '0dB in each band (flat function)', 'The frequency characteristic in each band is reversed with respect to 0dB (reverse function)'. - - - These functions can be software-controlled with one touch.
- Spectrum analyzing display can be used to provide recording equalization easily.
- Since 2 control lines can be also used for a display LSI, wiring between microcomputer and LSI is facilitated.

### Absolute Maximum Ratings at Ta = 25°C, VSS = 0V

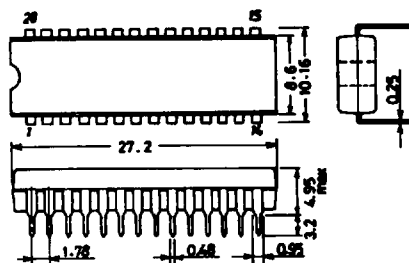
|                             | Pin Name | Conditions         |                        | unit |
|-----------------------------|----------|--------------------|------------------------|------|
| Maximum Supply Voltage      | VDD max  | VDD, VEE           | -8V ≤ VEE ≤ VSS ≤ VDD  | 16 V |
|                             | VEE max  | VDD, VEE           | -8V ≤ VEE ≤ VSS ≤ VDD  | 16 V |
|                             | VCC max  | VCC                | VSS to VSS + 7         | V    |
| Maximum Input Voltage       | V11      | CLK, DI            | 0 to VCC + 0.3         | V    |
|                             | V12      | f1 to f7, IN1, IN2 | VEE - 0.3 to VDD + 0.3 | V    |
|                             | V13      | S                  | VEE - 0.3 to VDD + 0.3 | V    |
|                             |          |                    |                        |      |
| Allowable Power Dissipation | Pd max   | Ta = 75°C          | 200                    | mW   |
| Operating Temperature       | Tpg      |                    | -30 to +75             | °C   |
| Storage Temperature         | Tstg     |                    | -40 to +125            | °C   |

### Pin Assignment



### Case Outline 3029A

(unit: mm)



SANYO: DIP28S

## LC7522

Recommended Operating Conditions at  $T_a = 25^\circ\text{C}$ ,  $V_{SS} = 0\text{V}$ 

|                | Pin Name | Conditions                                         |     | unit |
|----------------|----------|----------------------------------------------------|-----|------|
| Supply Voltage | $V_{DD}$ | $-7.0\text{V} \leq V_{EE} \leq V_{SS} \leq V_{DD}$ | 14  | V    |
|                | $V_{EE}$ | $-7.0\text{V} \leq V_{EE} \leq V_{SS} \leq V_{DD}$ | 14  | V    |
|                | $V_{CC}$ |                                                    | 5.0 | V    |

Allowable Operating Conditions at  $T_a = 25^\circ\text{C}$ ,  $V_{SS} = 0\text{V}$ ,  $V_{DD} \geq V_{CC}$ 

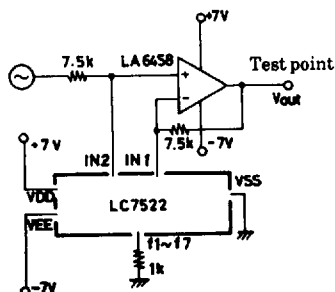
|                         | Pin Name            | Conditions                                                                     |                                             | unit          |
|-------------------------|---------------------|--------------------------------------------------------------------------------|---------------------------------------------|---------------|
| Supply Voltage          | $V_{DD}$            | $-7.5\text{V} \leq V_{EE} \leq V_{SS} \leq V_{DD}$                             | 7.5 to 15.0                                 | V             |
|                         | $V_{EE}$            | externally connect a capacitor of 1000pF or greater across $V_{DD} - V_{SS}$ . | 7.5 to 15.0                                 | V             |
|                         | $V_{CC}$            | $V_{CC} - V_{SS}$ and $V_{EE} - V_{SS}$ .                                      |                                             |               |
| Input 'H'-Level Voltage | $V_{IH1}$           | $V_{CC} \leq V_{DD}$                                                           | 4.5 to 5.5                                  | V             |
|                         | $V_{IH2}$           |                                                                                | $0.8V_{CC}$ to $V_{CC}$                     | V             |
|                         | $V_{IL1}$           |                                                                                | $0.9(V_{DD} - V_{EE}) + V_{EE}$ to $V_{DD}$ | V             |
| Input 'L'-Level Voltage | $V_{IL1}$           |                                                                                | $0.2V_{CC}$                                 | V             |
|                         | $V_{IL2}$           |                                                                                | $V_{EE}$ to $0.1(V_{DD} - V_{EE}) + V_{EE}$ | V             |
| Input Pulse Width       | $t_{\phi W}$        | CLK                                                                            | 1 min.                                      | $\mu\text{s}$ |
| Setup Time              | $t_{\text{set up}}$ | DI                                                                             | 1 min.                                      | $\mu\text{s}$ |
| Hold Time               | $t_{\text{hold}}$   | DI                                                                             | 1 min.                                      | $\mu\text{s}$ |
| Operating Frequency     | fopg                | CLK                                                                            | up to 330                                   | kHz           |

Electrical Characteristics at  $T_a = 25^\circ\text{C}$ 

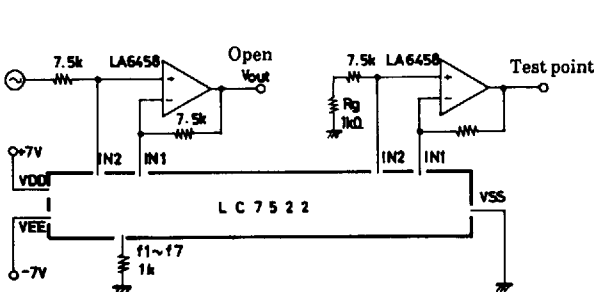
|                               | Pin Name   | Conditions                                                              | min | typ    | max   | unit          |
|-------------------------------|------------|-------------------------------------------------------------------------|-----|--------|-------|---------------|
| Total Harmonic Distortion     | THD 1      | $V_{OUT} = 1\text{V}$ , flat mode, $f = 20\text{kHz}$ , Test Circuit 1  |     | 0.005  | 0.01  | %             |
|                               | THD 2      | $V_{OUT} = 1\text{V}$ , flat mode, $f = 1\text{kHz}$ , Test Circuit 1   |     | 0.0015 | 0.003 | %             |
|                               | THD 3      | $V_{OUT} = 1\text{V}$ , boost mode, $f = 20\text{kHz}$ , Test Circuit 1 |     | 0.04   | 0.1   | %             |
|                               | THD 4      | $V_{OUT} = 1\text{V}$ , boost mode, $f = 1\text{kHz}$ , Test Circuit 1  |     | 0.015  | 0.03  | %             |
| Crosstalk between Channels    | Xtalk      | $V_{OUT} = 1\text{V}$ , $f = 20\text{kHz}$ , Test Circuit 2             |     | 55     |       | dB            |
| Setting Error                 | $\Delta B$ | Other band flat, $V_{DD} - V_{EE} = 14\text{V}$ , Test Circuit 1        | -1  |        | +1    | dB            |
| Current Dissipation           | $I_{DD}$   | $V_{DD} - V_{EE} = 15\text{V}$                                          |     |        | 1     | mA            |
|                               | $I_{CC}$   | $V_{CC} = 5\text{V}$                                                    |     |        | 1     | mA            |
| Analog SW OFF Leakage Current | $I_{OFF}$  | $f1$ to $f7$                                                            |     |        | 10    | $\mu\text{A}$ |

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Test Circuit 1



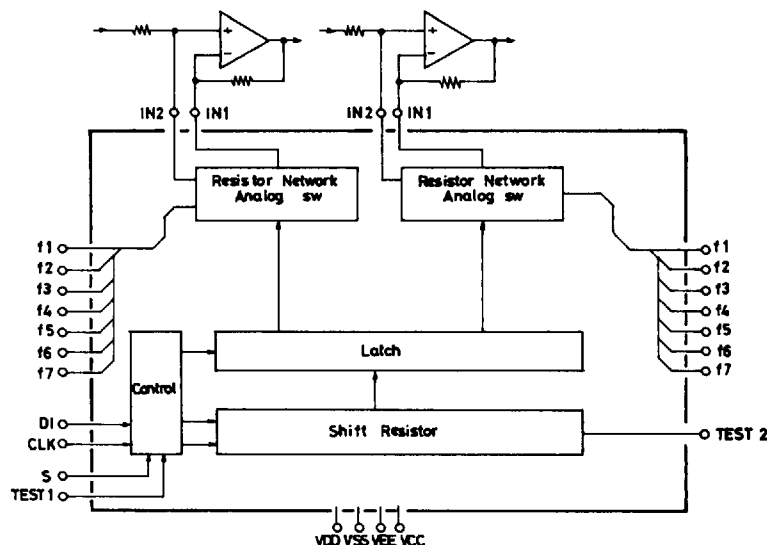
Test Circuit 2



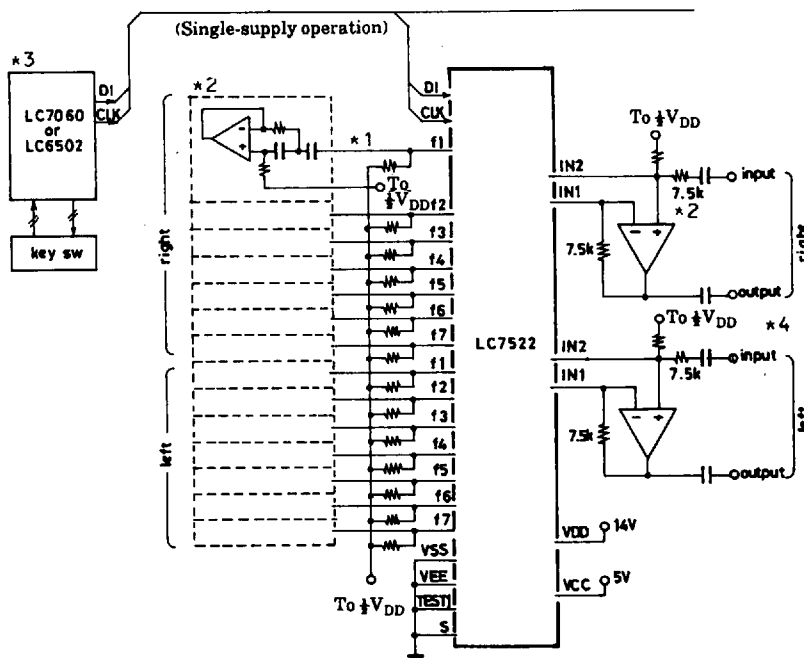
# LC7522

## Equivalent Circuit Block Diagram

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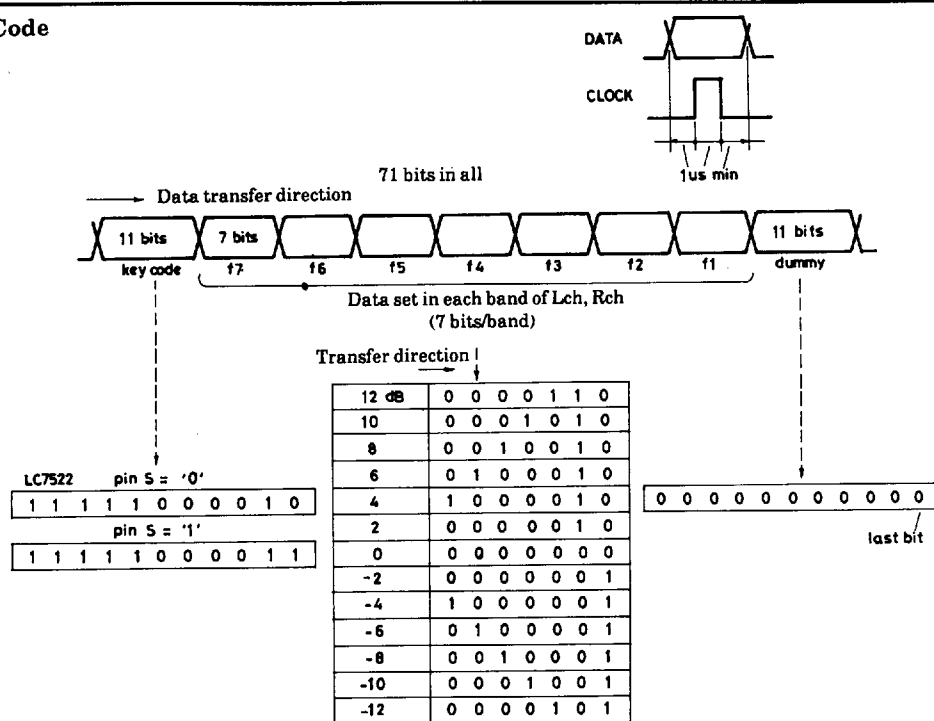
## Sample Application Circuit



- \*1 It is recommended that  $1/2V_{DD}$  is applied to pins f1 to f7 through resistors of  $1M\Omega$  so that noise is minimized at the select mode.
- \*2 The optimum conditions for 2dB/step are as follows :  
 $V_{DD} = 14V$ , feedback resistance of OP amp :  $7.5k\Omega$ , equivalent LC resonance impedance :  $1k\Omega$   
 (For  $V_{DD} = 8V$ , the LC7523 is recommended.)
- \*3 The LC7060 is available as a standard controller.
- \*4 The LC7560 (LCD driver), LC7565 (FLT, LED driver) are available as spectrum analyzing display drivers for graphic equalizer output signal.

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## Data Code



Note 1. When power is applied, data "0" must be first transferred for 60 clocks (initial clock) or more. If data transfer is stopped halfway, the transfer of the remaining data must be completed or data transfer must be started after the initial clocks have been transferred.

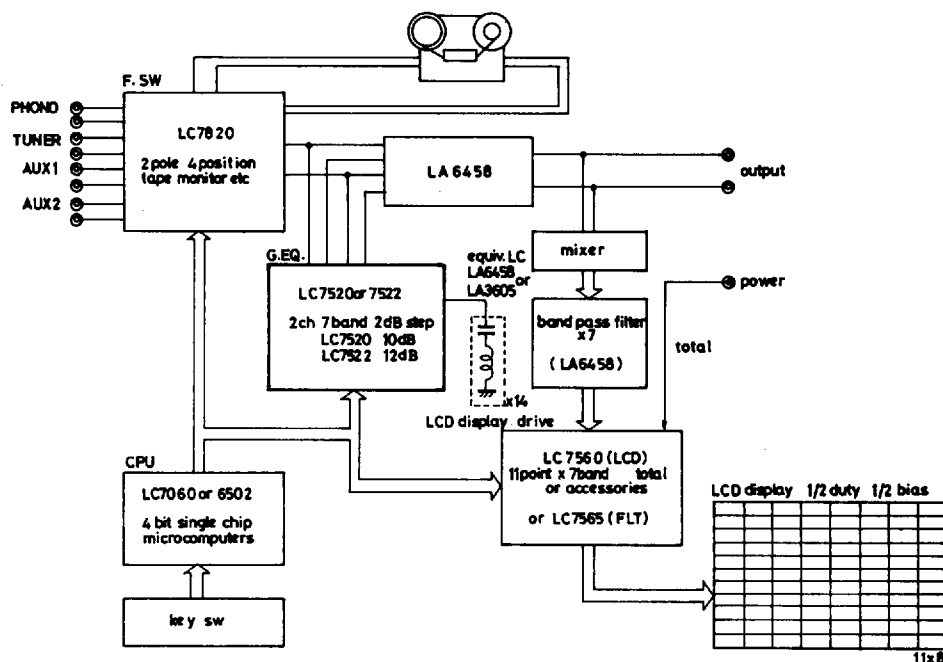
Note 2. When the DI, CLK pins are shared with the LC7560, etc., the maximum initial clocks for such device must be transferred.

## Pin Description

| Pin Name                                              | Pin Configuration | Description                                                                                                                                                                                                              |
|-------------------------------------------------------|-------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| V <sub>DD</sub><br>V <sub>SS</sub><br>V <sub>EE</sub> |                   | Power supply pin +7V typ. power supply for audio signal<br>Power supply pin 0V<br>Power supply pin -7V typ. power supply for audio signal, connected to V <sub>SS</sub> at single-supply operation                       |
| V <sub>CC</sub>                                       |                   | Power supply pin +5V typ.                                                                                                                                                                                                |
| DI                                                    |                   | Used to input data from CPU<br>Schmitt inverter type                                                                                                                                                                     |
| CLK                                                   |                   | Used to input clock from CPU<br>Schmitt inverter type                                                                                                                                                                    |
| IN1<br>IN2                                            |                   | Audio signal input pin<br>Normally, IN1 is connected to inverting input of OP amp.<br>Normally, IN2 is connected to noninverting input of OP amp.<br>Provided in Lch/Rch                                                 |
| f1 to f7                                              |                   | Band-pass filter connecting pin<br>f1 to f7 × 2 (right/left) = 14(total) pins                                                                                                                                            |
| S                                                     |                   | Select pin at 2-chip used mode<br>To accept data under key code 7C3, S must be set to '1'.<br>→Connected to V <sub>DD</sub><br>To accept data under key code 7C2, S must be set to '0'.<br>→Connected to V <sub>EE</sub> |
| TEST1<br>TEST2                                        |                   | IC test pin<br>Open during operation                                                                                                                                                                                     |

## LC7522

[Reference 1] ECS System/Graphic Equalizer Application Circuit Block Diagram



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[Reference 2] Main Specifications for LC7060 (CMOS LSI/Graphic Equalizer Controller)

### Use

Controller LSI for graphic equalizer electronic volume control LSI : LC7520,7522, LCD driver : LC7560, FLT driver : LC7565.

### Functions

- 7 bands, 2dB/step,  $\pm 10\text{dB}$  ( $\pm 12\text{dB}$ ) variable, ( ): LC7522/7565-combined use.
- Max. 8 memories (user option 5 modes, maker option 3 modes) + last channel memory.
- Possible to control function switch (5 positions) and electronic volume control.
- 2 control lines for graphic equalizer electronic volume control and display IC
- Buzzer sound is generated when a key is operated.
- On-chip remote control reception program.

### Features

- Any combination of graphic equalizer electronic volume control LSI LC7520,7522, and display driver LSI LC7560,7565 may be used. (Port-selectable)
- FLAT function to permit the FLAT mode to be entered with one touch.
- REVERSE function to permit the frequency characteristic to be reversed with respect to 0dB with one touch.
- Tuner band select and SCAN output.
- MUTE and MUTE output.
- Backup operation available.