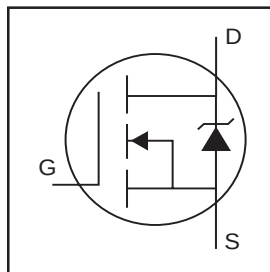


IRFB9N60A

HEXFET® Power MOSFET

- Dynamic dv/dt Rating
- Repetitive Avalanche Rated
- Fast Switching
- Ease of Paraleling
- Simple Drive Requirements

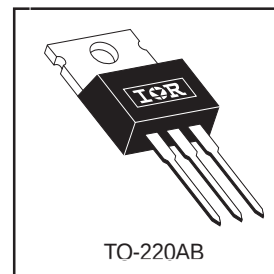


$V_{DSS} = 600V$
 $R_{DS(on)} = 0.75\Omega$
 $I_D = 9.2A$

Description

Third Generation HEXFETs from International Rectifier provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The TO-220 package is universally preferred for all commercial-industrial applications at power dissipation levels to approximately 50 watts. The low thermal resistance and low package cost of the TO-220 contribute to its wide acceptance throughout the industry.



Absolute Maximum Ratings

	Parameter	Max.	Units
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	9.2	A
$I_D @ T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	5.8	
I_{DM}	Pulsed Drain Current ①	37	
$P_D @ T_C = 25^\circ C$	Power Dissipation	170	W
	Linear Derating Factor	1.3	W/°C
V_{GS}	Gate-to-Source Voltage	± 30	V
E_{AS}	Single Pulse Avalanche Energy②	290	mJ
I_{AR}	Avalanche Current①	9.2	A
E_{AR}	Repetitive Avalanche Energy①	17	mJ
dv/dt	Peak Diode Recovery dv/dt ③	5.0	V/ns
T_J	Operating Junction and	-55 to + 150	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting torque, 6-32 or M3 screw	10 lbf•in (1.1N•m)	

Thermal Resistance

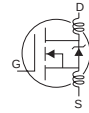
	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	0.75	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.50	—	
$R_{\theta JA}$	Junction-to-Ambient	—	62	

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Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	600	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.66	—	V/ $^\circ\text{C}$	Reference to 25°C , $I_D = 1\text{mA}$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.75	Ω	$V_{GS} = 10V, I_D = 5.5A$ ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
g_{fs}	Forward Transconductance	5.5	—	—	S	$V_{DS} = 25V, I_D = 5.5A$
I_{DSS}	Drain-to-Source Leakage Current	—	—	25	μA	$V_{DS} = 600V, V_{GS} = 0V$
		—	—	250		$V_{DS} = 480V, V_{GS} = 0V, T_J = 150^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 30V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -30V$
Q_g	Total Gate Charge	—	—	49	nC	$I_D = 9.2A$
Q_{gs}	Gate-to-Source Charge	—	—	13		$V_{DS} = 400V$
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	—	20		$V_{GS} = 10V$, See Fig. 6 and 13 ④
$t_{d(on)}$	Turn-On Delay Time	—	13	—	ns	$V_{DD} = 300V$
t_r	Rise Time	—	25	—		$I_D = 9.2A$
$t_{d(off)}$	Turn-Off Delay Time	—	30	—		$R_G = 9.1\Omega$
t_f	Fall Time	—	22	—		$R_D = 35.5\Omega$, See Fig. 10 ④
L_D	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact
L_S	Internal Source Inductance	—	7.5	—		
C_{iss}	Input Capacitance	—	1400	—	pF	$V_{GS} = 0V$
C_{oss}	Output Capacitance	—	180	—		$V_{DS} = 25V$
C_{rss}	Reverse Transfer Capacitance	—	7.1	—		$f = 1.0\text{MHz}$, See Fig. 5
C_{oss}	Output Capacitance	—	1957	—		$V_{GS} = 0V, V_{DS} = 1.0V, f = 1.0\text{MHz}$
C_{oss}	Output Capacitance	—	49	—		$V_{GS} = 0V, V_{DS} = 480V, f = 1.0\text{MHz}$
$C_{oss \text{ eff.}}$	Effective Output Capacitance ⑤	—	96	—		$V_{GS} = 0V, V_{DS} = 0V \text{ to } 480V$



Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	9.2	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	37		
V_{SD}	Diode Forward Voltage	—	—	1.5	V	$T_J = 25^\circ\text{C}, I_S = 9.2A, V_{GS} = 0V$ ④
t_{rr}	Reverse Recovery Time	—	530	800	ns	$T_J = 25^\circ\text{C}, I_F = 9.2A$
Q_{rr}	Reverse Recovery Charge	—	3.0	4.4	μC	$di/dt = 100A/\mu s$ ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S + L_D$)				

Notes:

① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)

② Starting $T_J = 25^\circ\text{C}$, $L = 6.8\text{mH}$
 $R_G = 25\Omega$, $I_{AS} = 9.2A$. (See Figure 12)

③ $I_{SD} \leq 9.2A$, $di/dt \leq 50A/\mu s$, $V_{DD} \leq V_{(BR)DSS}$,
 $T_J \leq 150^\circ\text{C}$

④ Pulse width $\leq 300\mu s$; duty cycle $\leq 2\%$.

⑤ $C_{oss \text{ eff.}}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}

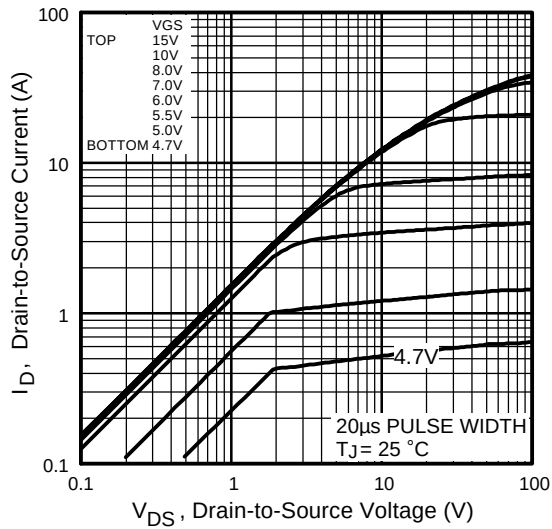


Fig 1. Typical Output Characteristics

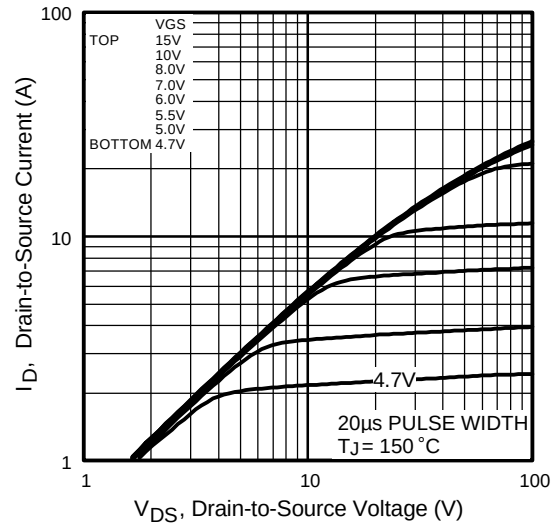


Fig 2. Typical Output Characteristics

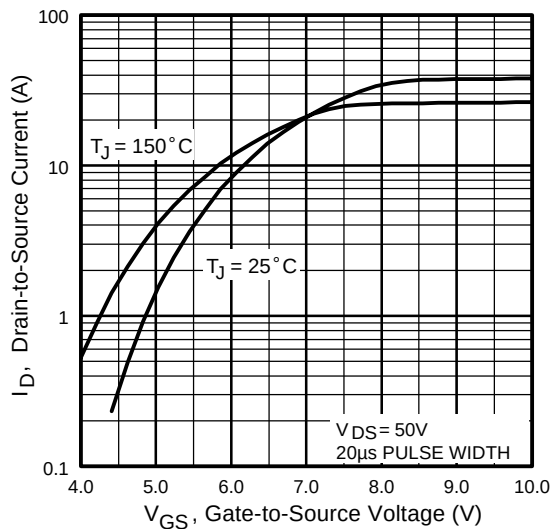


Fig 3. Typical Transfer Characteristics

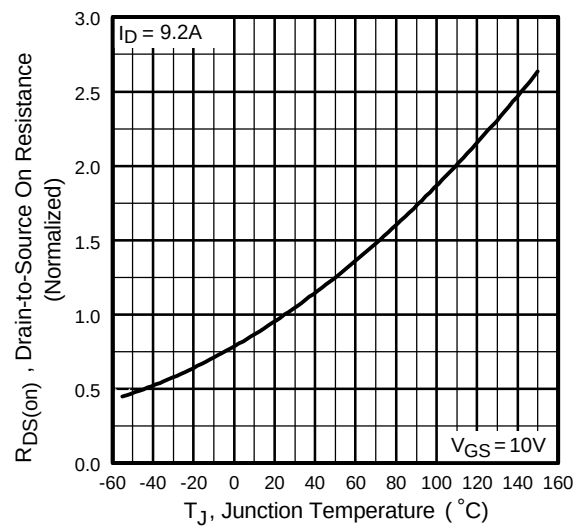


Fig 4. Normalized On-Resistance Vs. Temperature

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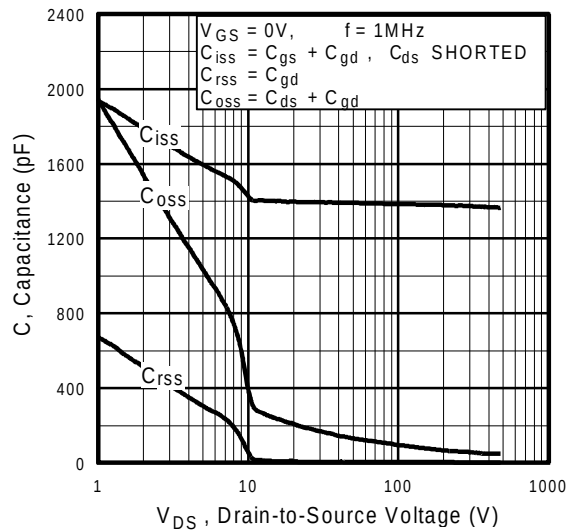


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

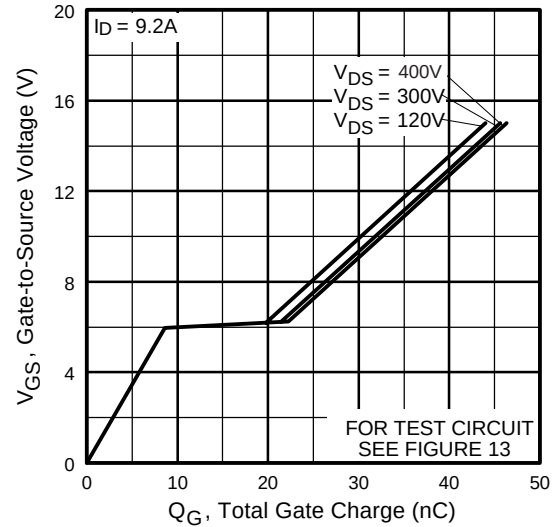


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

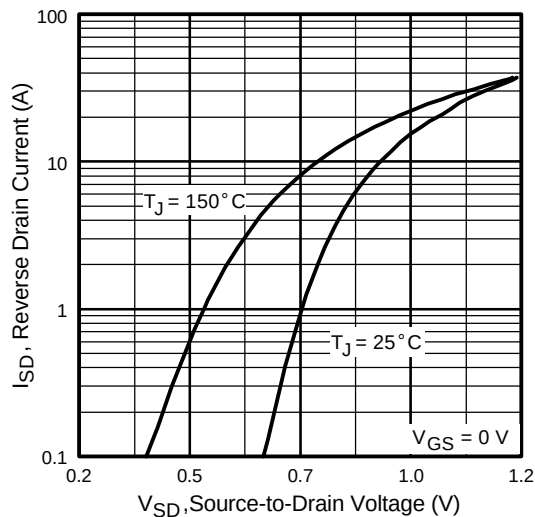


Fig 7. Typical Source-Drain Diode Forward Voltage

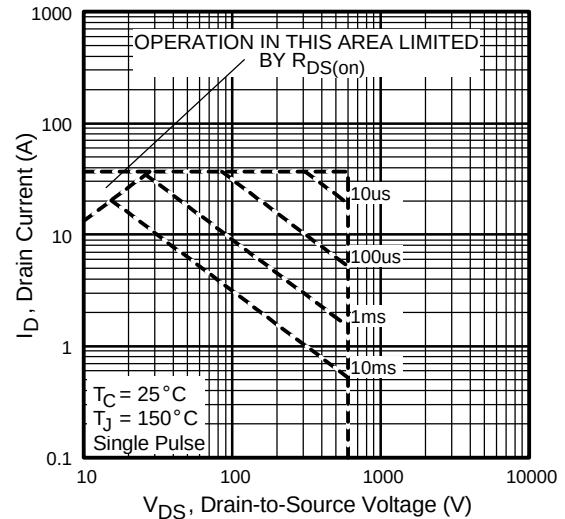


Fig 8. Maximum Safe Operating Area

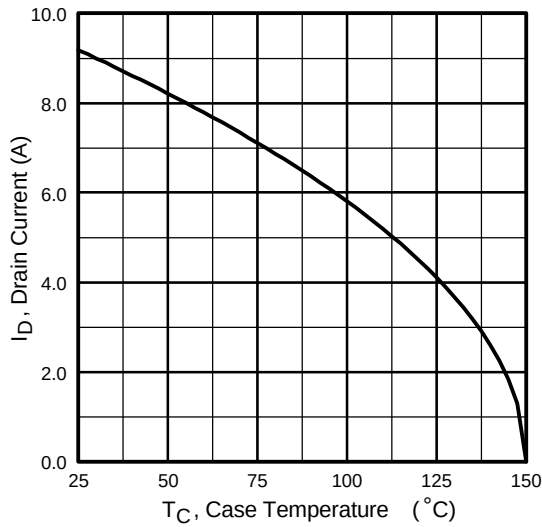


Fig 9. Maximum Drain Current Vs. Case Temperature

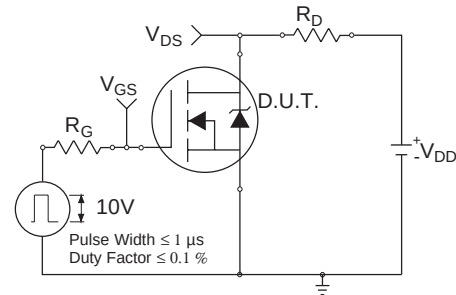


Fig 10a. Switching Time Test Circuit

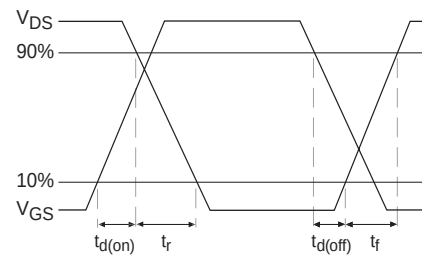


Fig 10b. Switching Time Waveforms

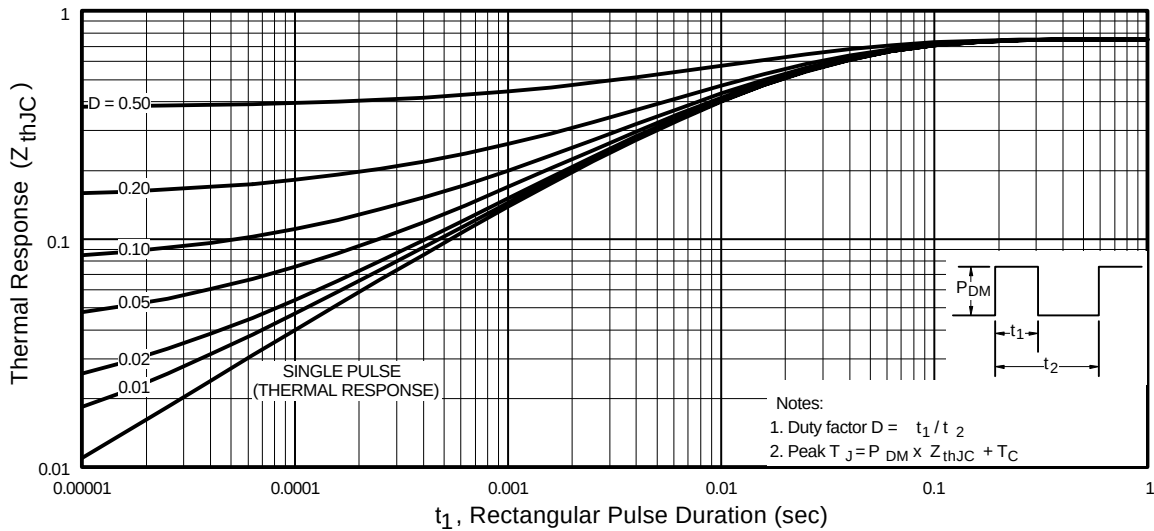


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

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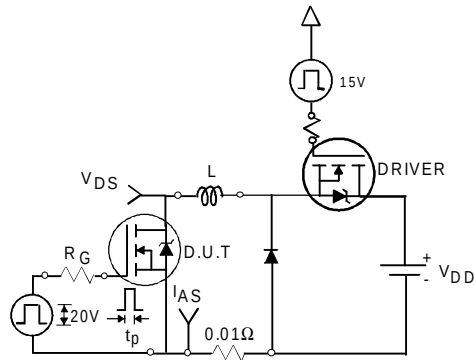


Fig 12a. Unclamped Inductive Test Circuit

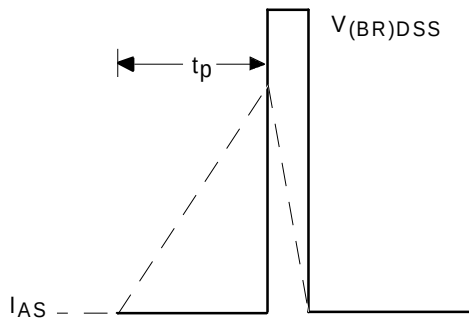


Fig 12b. Unclamped Inductive Waveforms

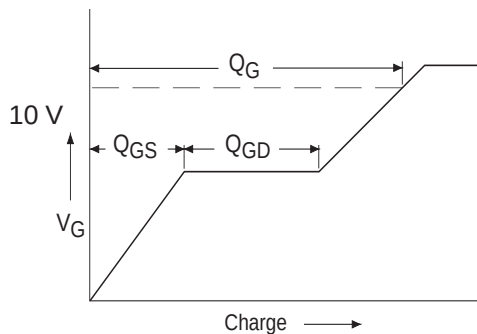


Fig 13a. Basic Gate Charge Waveform

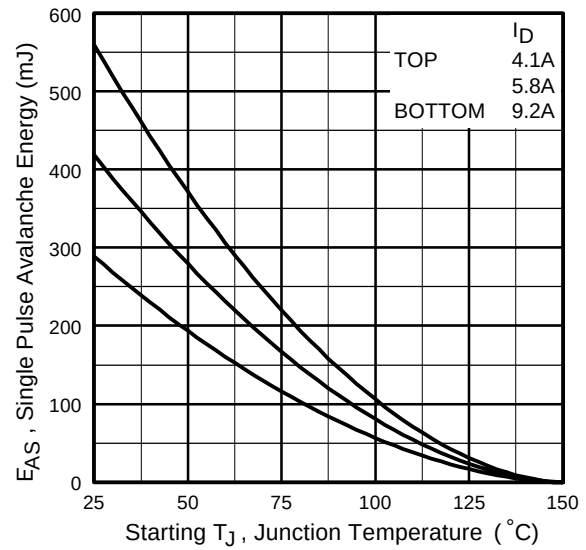


Fig 12c. Maximum Avalanche Energy
Vs. Drain Current

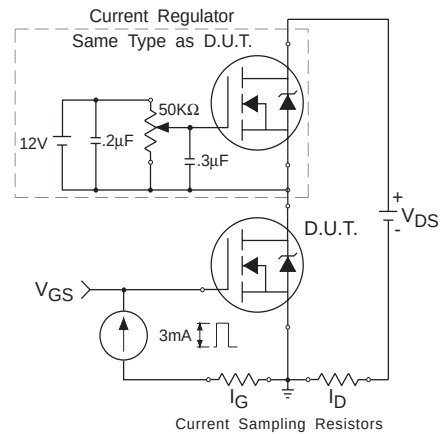
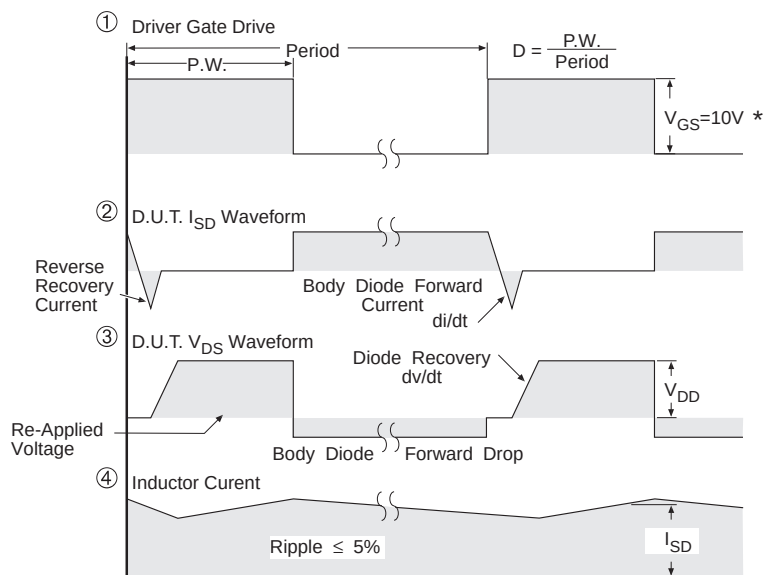
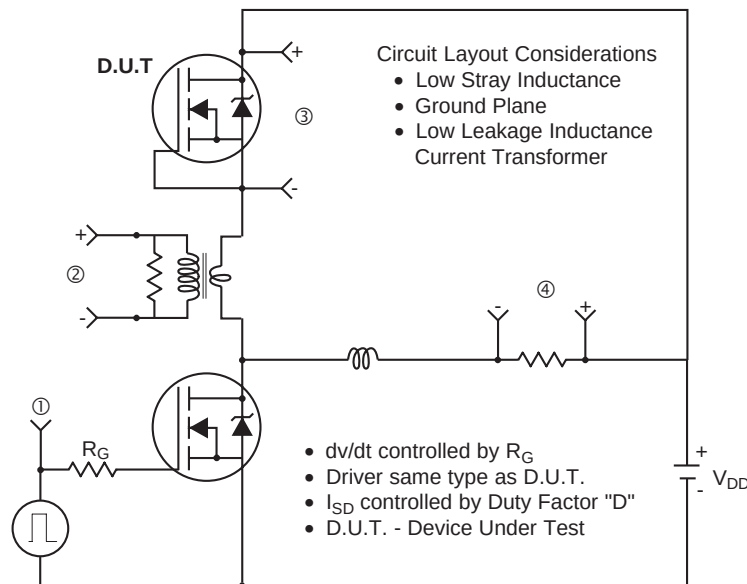


Fig 13b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit



* $V_{GS} = 5V$ for Logic Level Devices

Fig 14. For N-Channel HEXFETS

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TO-220AB Outline

The drawing shows a 3-pin TO-220AB package. The front view (left) includes dimensions for the body, pins, and mounting tab. The side view (right) shows the lead profile and mounting tab dimensions. A lead assignment legend is provided on the right.

LEAD ASSIGNMENTS

- 1 - GATE
- 2 - DRAIN
- 3 - SOURCE
- 4 - DRAIN

NOTES:

- 1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
- 2 CONTROLLING DIMENSION : INCH
- 3 OUTLINE CONFORMS TO JEDEC OUTLINE TO-220AB.
- 4 HEATSINK & LEAD MEASUREMENTS DO NOT INCLUDE BURRS.

TO-220AB

Diagram illustrating the markings on an IRF1010 MOSFET package:

- INTERNATIONAL RECTIFIER LOGO**: Points to the "IR" logo.
- PART NUMBER**: Points to "1010".
- DATE CODE (YYWW)**: Points to "9246".
 - YY = YEAR
 - WW = WEEK
- ASSEMBLY LOT CODE**: Points to "9B 1M".

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<http://www.irf.com/> Data and specifications subject to change without notice. 10/98